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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,176	12/04/2003	Rose Mulligan	42P16008	8588
8791	7590	06/01/2005	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN			KIELIN, ERIK J	
12400 WILSHIRE BOULEVARD			ART UNIT	
SEVENTH FLOOR			PAPER NUMBER	
LOS ANGELES, CA 90025-1030			2813	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/729,176		MULLIGAN, ROSE	
	<b>Examiner</b>		<b>Art Unit</b>	
	Erik Kielin		2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) none is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,5,6 and 8-13 is/are rejected.
- 7) ☒ Claim(s) 3,4,7 and 14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication 2004/0232524 A1 (**Howard et al.**).

Regarding **claim 1**, **Howard** discloses, a process comprising:

dicing a semiconductor wafer before forming devices on the semiconductor wafer

(paragraph [0015]), the dicing forming trenches **107** in the semiconductor wafer **100** by etching

(paragraph [0017]) --as further limited by instant **claim 5**;

forming an oxide in the trenches formed by dicing the semiconductor wafer --as further limited by instant **claim 2** (paragraph [0025]);

forming the semiconductor devices on the diced semiconductor wafer (paragraph [0026]);

removing the oxide from the trenches after the devices are formed (paragraph [0027]);

back-grinding the semiconductor wafer after forming the devices on the semiconductor wafer (paragraphs [0052] and [0056]).

*Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6 and 8-10 rejected under 35 U.S.C. 103(a) as being unpatentable over **Howard**.

The prior art of **Howard**, as explained above, discloses each of the claimed features except for indicating the depth of the trenches is 90 to 150 microns from the surface of the semiconductor wafer. **Howard** does however teach,

“[0018] Depth 105a and width 107 of the trench are correlated by the aspect ratio depth-to-width, which is achievable by the selected etching technique. For plasma etching technology, the aspect ratio is preferably 8:1 or less (such as 6:1 or 4:1). As an example, a trench depth of 20  $\mu\text{m}$  would require a trench width of approximately 2 to 3  $\mu\text{m}$ . For shallower trenches, a trench width of about 1  $\mu\text{m}$  or even 0.5  $\mu\text{m}$  is achievable.”

And regarding the embodiments wherein backside grinding is used to form the trenches 107, **Howard** states in paragraph [0046],

“in this embodiment, the trench streets may have to be etched deeper than in the previously described embodiments, since the trench streets have to penetrate the whole depth of the intended final wafer thickness”

Accordingly, the depth of the trench can be optimized depending upon the method of forming the trenches. In this regard, it has been held that

“Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree

from the results of the prior art... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality .... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller* 105 USPQ233, 255 (CCPA 1955).

See also *In re Waite* 77 USPQ 586 (CCPA 1948); *In re Scherl* 70 USPQ 204 (CCPA 1946); *In re Irmischer* 66 USPQ 314 (CCPA 1945); *In re Norman* 66 USPQ 308 (CCPA 1945); *In re Swenson* 56 USPQ 372 (CCPA 1942); *In re Sold* 25 USPQ 433 (CCPA 1935); *In re Dreyfus* 24 USPQ 52 (CCPA 1934).

According to precedent, then, and the teachings in **Howard**, the choice of trench depth is a matter of routine optimization, and one of ordinary skill would be motivated to use the depth of 90  $\mu\text{m}$  to 150  $\mu\text{m}$  in order to form a trench of optimum depth and to avoid the saw from coming too close to the electronic devices formed in the semiconductor wafer.

5. Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Howard** as applied to claims 8-10 above, and further in view of US 5,414,297 (**Morita et al.**).

The prior art of **Howard**, as explained above, discloses each of the claimed features except for indicating that the oxide filling the trench is planarized.

**Morita** teach forming and planarizing an insulating film 46 in "along the entirety of the scribe line 2" before forming the semiconductor devices and singulating the wafer in to dice (Figs. 2a-2e; Title; Abstract; col. 9, lines 20-54).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to make the oxide fill of **Howard** planar, in order to correct any unevenness in height prior to

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formation of the semiconductor devices, as taught by **Morita**. A planar topography aids alignment of the wafer for subsequently deposited device layers.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Howard** in view of **Mortia** as applied to claims 8-11 above, and further in view of US 5,716,495 (**Butterbaugh et al.**

The prior art of **Howard** in view of **Mortia**, as explained above, discloses each of the claimed features except that Howard does not indicate how the oxide in the trench is removed.

**Butterbaugh** teaches the benefits of using a UV laser to remove oxide and contaminants from a semiconductor wafer with good control of the endpoint.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a UV laser to remove the oxide of **Howard**, because **Howard** is silent to the method of removing the oxide such that one of ordinary skill would be motivated to use known methods that have additional benefits such as removing contaminants, such as that taught in **Butterbaugh**.

*Allowable Subject Matter*

7. Claims 3, 4, 7, and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 3 and 14, the prior art does not teach or suggest, in combination with the other claimed limitations, the method of singulating a wafer into dice by forming a trench in

the semiconductor wafer, itself, by dicing before any devices are formed thereon, scribing the trench, and finally backside grinding to separate the wafer in to dice.

Claims 4 and 7 depend from claim 3 and therefore have all of the limitations of claim 3. Given that the trench in Howard is clearly sufficient to separate the wafer by backside grinding, the step of scribing the trench in Howard would be superfluous and therefore at best obvious to try.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached from 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erik Kielin  
Primary Examiner  
May 27, 2005